A New Junction Technology for Low-Resistance Contacts and Schottky Barrier MOSFETs

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***Abstract*:** By imposing an ultra-thin insulator between low-workfunction metals and silicon, the Schottky barrier of the junction can be substantially reduced, reducing junction resistance. With this approach, low Schottky barrier metal S/D MOSFETs with Mg and Yb as S/D metals are demonstrated.

I. Introduction

The challenges for engineering the source and drain (S/D) regions of advanced CMOS are increasingly severe. The drive to shallower junctions requires extreme technology to control the dopant depth and profile, while simultaneously limiting the resistance to acceptable values. One approach to managing short-channel integrity is ultra-thin-body fully-depleted SOI technology. However, doped S/D's in ultra-thin Si suffer from excessive sheet resistance, resulting in high resistance from the channel to the silicide contact, and high contact resistance to the silicide. One approach to improving sheet resistance is elevated S/D technology. However, this adds a penalty in gate-to-drain and gate-to-source capacitance, and the issue of doping control remains. The obvious solution is metal, or "Schottky", S/D. Yet Schottky S/D MOSFETs, especially n-channel MOSFETs, have to date been generally limited by excessive Schottky barriers between the S/D and the channel.

In this paper, we present a new junction technology between a metal and a semiconductor. The result is a low-resistance contact that may be used for contacts to doped S/D regions as well as to replace the doped S/D regions with a metal for advanced high-performance Schottky barrier MOSFETs. The technology, which involves inserting an ultra-thin insulator between the metal and the semiconductor, lowers the Schottky barrier and *reduces the resistance*, by a factor of 5000 in Mg contacts to moderately-doped n-type Si.

II. Junction Technology

The key to the new junction technology is to insert an ultra-thin insulator between the metal and the semiconductor [1]. This has the effect of lowering the Schottky barrier, which can result in lower junction resistance if the insulator is not too thick. That is, adding the insulator has two effects on resistance: the Schottky barrier may be lower, decreasing resistance; and the insulator adds resistance, yet current still flows due to tunneling. Thus, the junction resistance is a competition between lower Schottky barrier and higher tunneling resistance.

The optimal thickness for the insulator is likely around 3-5 Å. The tunneling resistance of an insulator is a strong function of the insulator thickness. For example, using an abrupt band approximation to Si/Si_3N_4/Si, tunneling resistance between the Si conduction bands varies by a decade for each 2.6 Å increase in the Si_3N_4 thickness [2]. This relationship will be somewhat different for other electrode materials, non-stoichiometric Si_xN_y, and for films of insufficient thickness to establish a bulk-like band structure. Nevertheless, it is clear that the optimal insulator thickness exists in a range of only a few Å. That is, as the insulator thickness increases from zero, the resistance of a junction will drop very sharply then increase again. Thus, to observe this effect the precise thickness control available in modern semiconductor manufacturing methods must be utilized.

The Schottky barrier is reduced because the Fermi level of the metal is depinned with the insulator (Fig. 1). That is, the Fermi level of a metal in contact with a semiconductor is the result of an interplay between the bulk workfunction of the metal Φ_M and surface states of the semiconductor. The Fermi level of the metal tends to align, or "pin", near the "charge neutral level" of the semiconductor, within the semiconductor band gap. The final pinning point, the effective workfunction Φ_{eff}, is crudely proportional to the difference between the "bulk" workfunction of the metal and the semiconductor charge neutral level. The proportionality constant is material-dependent, given by the depinning factor [3]:

$$S = d\phi_{eff} / d\phi_M \,. \qquad (1)$$

The effective workfunction is then

$$\phi_{eff} = \phi_{pin} + S(\phi_M - \phi_{pin}) \,. \qquad (2)$$

Generally, the depinning factor is greater the larger the semiconductor or insulator band gap. For example, values of S = 0.17 for Si, 0.55 for Si_3N_4, and 0.9 for SiO_2 have been reported [4]. One proposed explanation for such a relation is intrinsic metal induced gap states (MIGS), a quantum mechanical effect present at all MS interfaces [5]. The MIGS, and hence the pinning, are still present even when extrinsic defect states, such as dangling bonds, are removed from the interface. In Si, the charge neutral level has been reported to be approximately Φ_{pin} = 4.7 V relative to the vacuum potential [3].

The new junction technology utilizes the larger depinning factor for insulators in combination with a low (high) workfunction metal, to align the Fermi level of a metal with the conduction (valence) band of a semiconductor. An interfacial insulator of even a few monolayers is sufficient to reduce the metal/semiconductor interaction, reducing the Schottky barrier height of metal/semiconductor contacts.

III. Results: Contacts

We have measured a wide range of metals in contacts to Si with silicon nitride as the insulator. The nitrides are grown with a low-energy N source at elevated temperatures in UHV, and the metal is deposited *in situ*. A cross-sectional TEM (Fig. 2) shows an example of a thin nitride. An important factor in these films is uniformity. The film in the figure appears to have non-uniform thickness, yielding an inhomogeneous interface. Consequently, current may be dominated by regions somewhat thinner than the mean.

Fig. 3 shows the example of $Al/Si_3N_4/n^+$ Si. The sharp drop in resistance as a function of thickness is demonstrated by changing the growth time of the nitride. The resistance drops at short growth times due to depinning, then increases again at longer growth times due to tunneling resistance. The slow rise with time is possibly due to slowed growth of the nitride. This experiment also demonstrates the degree of nitride thickness control is at least sufficient to substantially reduce the resistance of the contact, although as was shown in Fig. 2, there is room for further improvement.

In Mg contacts, for example, the effect of an insulator is quite dramatic (Fig. 4). Here, the conductance of the contact with the nitride increases by a factor of 5000. The result is consistent with Synopsys/DESSIS [6] simulations of a barrier height of 0.16 V, a drop of 0.22 V relative to the case where no interfacial insulator is used. Fig. 5 shows typical conductance-versus-voltage plots, both measured and simulated. There is a small anomaly in the simulated curve as the diode undergoes a transition from reverse to forward bias. However, the agreement between simulation and experiment, especially in the higher-barrier case of no interfacial nitride, is encouraging.

Lower workfunction metals have also been measured. For example, in Er/Si_3N_4/p-type Si diodes (Fig. 6), results were consistent with DESSIS simulations of a band offset between the Er and the Si conduction band of only 45 mV. Measuring the offset on p-type Si makes a highly rectifying junction, as opposed to a nearly ohmic one, reducing the influence of substrate resistance. The dielectric thickness of the interfacial nitride layer implies that there is an electric field dependence to the effective barrier height. Thus, a difference between values extracted on n-type and p-type substrates is expected.

Junctions with no, or a sub-optimaly thick interfacial layer exhibit Schottky-limited behavior, and are well modeled as a metal/semiconductor contact. However, as the interfacial layer becomes thick enough for tunneling resistance to dominate, the metal/semiconductor contact models do not accurately reproduce the observed conductance versus junction voltage. Between the Schottky-limited and tunneling-limited regimes, the substrate resistance may be the limiting factor. Therefore, reducing the influence of the substrate resistance is critical to improving experimental resolution. One approach, used here, is to apply current to an anode, measure the applied voltage with a separate probe, and measure voltage on the other side of the junction from a nearby "tap" contact [1].

This approach helps, but to maximize resolution of contact resistance, nanoscale contacts are needed. Simulations show that, for a circular contact on a thick substrate, assuming contact resistance inversely proportional to the contact area, the ratio of contributions to the total resistance from the contact and from the substrate can be approximated as

$$\frac{R_c}{R_s} = \frac{4}{\pi r_c}\frac{\rho_c}{\rho_s}\,. \tag{3}$$

In the equation, R_c is the resistance from the contact, R_s is the resistance from the substrate, ρ_c is the specific contact resistivity, ρ_s is the substrate resistivity, and r_c is the contact radius. For example, consider a heavily-doped substrate with $\rho_s = 20\ \Omega$-µm, for which one wishes to resolve a specific contact resistivity of $\rho_c = 1\ \Omega\text{-}\mu m^2$. Then, for a substrate contribution to the resistance of no greater than the contribution from the contact, the radius of the contact must be at most approximately 60 nm. Future experiments will use small contacts and optimized substrate doping to improve the resolution of diode experiments.

IV. Results: MOSFETs

To demonstrate this junction technology in transistors, we have fabricated back-gated Schottky barrier MOSFETs on SOITEC SOI wafers where the buried oxide serves as the gate insulator. A schematic cross-section is shown in Fig. 7. Critical dimensions include a buried oxide (the gate oxide) thickness of 16 nm and a Si body thickness of 5.6 nm. All Si was doped approximately 10^{15}/cm^3 p-type.

The first devices with Yb, in which the nitride thickness has not been optimized, show a dramatic increase in drive current compared to a control device with no nitride (Figs. 8 & 9). The minimum drain current of the Yb/Si_3N_4/Si S/D $L = 2$ μm FET is only 10 pA/μm at $V_D = 2$ V, demonstrating the technology is compatible with low-standby-power off-state leakage current requirements.

Devices using Mg show similar performance (Fig. 10). Results are consistent with DESSIS simulations with a S/D barrier height of 0.20 V.

Interestingly, Mg yielded better results than some lower-workfunction metals. There are many factors that may contribute to this, including a non-optimized nitride thickness, chemically-induced interface dipoles [7], and deviations from the simplistic linear Fermi level pinning model, including *d*-shell interactions from transition metals [8].

A weakness of the device structure is a lack of "gate" doping. Thus, while the "gate" (substrate) is accumulated for sufficiently positive gate voltage, in weak inversion the gate becomes depleted, an effect enhanced by high interface state densities. Sufficiently below threshold, the gate inverts, restoring gate control of the channel. In future runs, the substrate will be implanted, and FGA-compatible S/D metals will be investigated, to improve the characteristics of these transistors.

V. Future Directions and Conclusions

Work is ongoing to improve the resolution of the specific contact resistance to determine the ultimate limits of this technology. Smaller contacts and optimized Schottky barrier MOSFETs are likely to yield improved results.

A limiting factor to practical devices is the low thermal budget of the Yb and Mg interfaces. Both metals are highly reactive and temperatures as low as 200 C increase the effective Schottky barrier height of the interface, perhaps due to chemical reaction. We are currently exploring materials with low workfunction and improved thermal stability.

In summary, we have developed a new junction technology that results in low-barrier Schottky contacts. This is achieved by inserting an ultra-thin insulator at the interface of a metal/semiconductor contact. The advantage of this technology is evident only over a narrow range of insulator thickness, which is accessible with modern manufacturing techniques. These innovative junctions may afford low resistance contacts to Si as well as enable high-performance metal S/D Schottky barrier MOSFETs.

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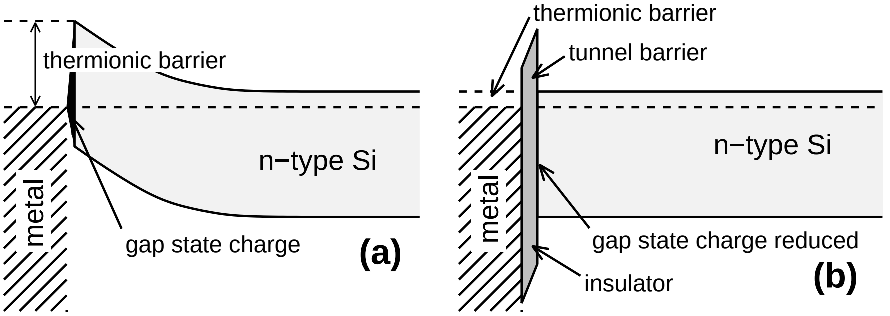

Fig. 1: Schematic band diagram of metal/n-type Si interface (a) without, and (2) with an ultra-thin interfacial insulator. The insulator reduces the gap state density, depinning the Fermi level, reducing the thermionic barrier.

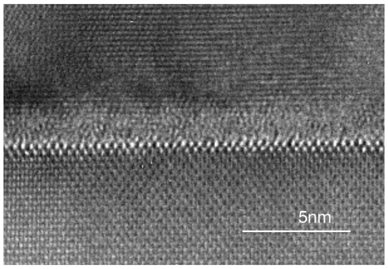

Fig. 2: Transmission electron micrograph (TEM) of a Ti/Si_3N_4/Si stack using the thermal nitride process used in this work. There is evidence of a non-uniform nitride thickness, implying further process optimization is possible.

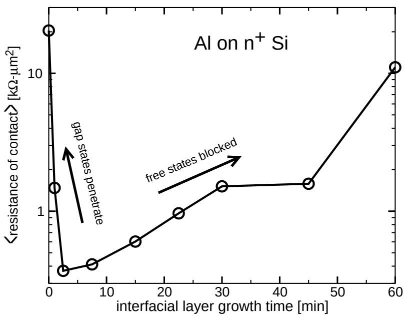

Fig. 3: “V-curve” showing the effect of interfacial nitridation time on junction resistance, for Al on n$^+$ Si. The minimum resistance balances gap state passivation and tunneling resistance through the interfacial layer.

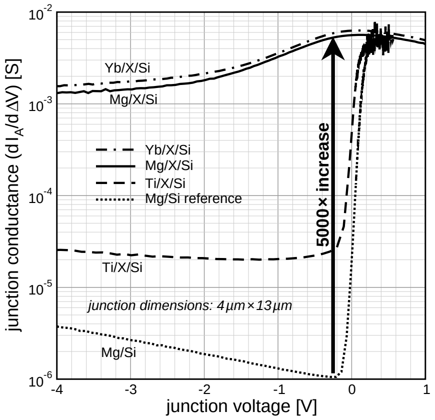

Fig. 4: Incremental conductance versus voltage for metal/semiconductor junctions with or without interfacial nitride layers (“X”). Mg experiences a 5000× increase with the interfacial “X” layer.

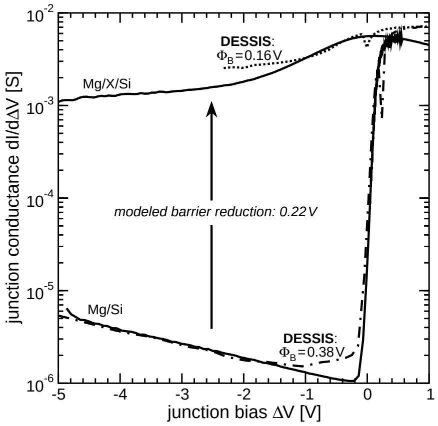

Fig. 5: Comparison of DESSIS simulations to measured data for Mg/n-type Si and Mg/Si$_3$N$_4$/n-type Si junctions. Results are consistent with the nitride layer reducing the effective barrier height by 0.22 V without notably increasing resistance at small forward bias.

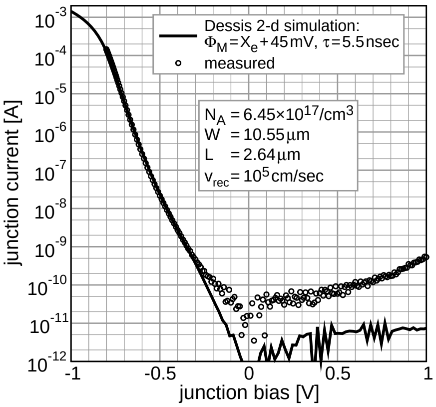

Fig. 6: Junction current versus voltage for Er/Si$_3$N$_4$/p-type Si diodes, comparing measured data to DESSIS simulations with a metal workfunction 45 mV greater than the Si electron affinity.

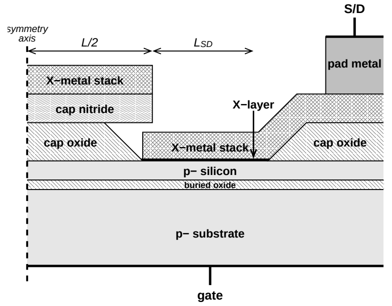

Fig. 7: Schematic half cross-section of back-gated transistor. The “X-layer” is the interfacial nitride. The “X-metal stack” is a low workfunction metal, such as Mg or Yb, capped with a protective layer, such as Ti or Al. $L_{SD} \approx 5$ µm.

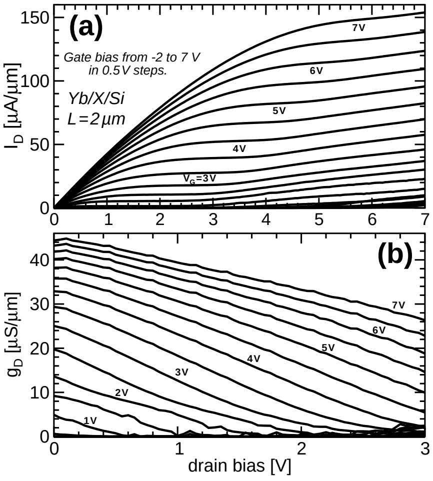

Fig. 8: (a) I_D versus V_D of Yb/Si$_3$N$_4$/Si S/D back-gated MOSFET. (b) Output conductance versus drain voltage for same transistor. Note the lack of low-voltage decrease in the output conductance and strong gate control of the conductance through the entire gate voltage range.

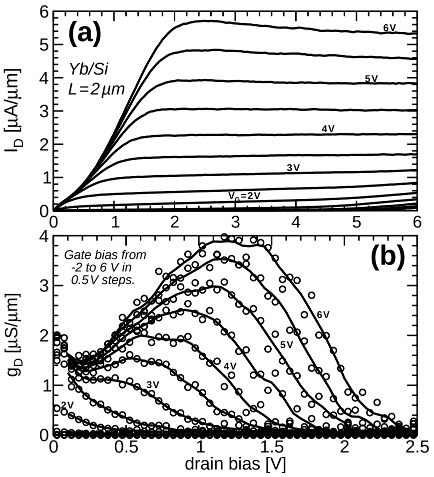

Fig. 9: I_D versus V_D of Yb/Si S/D back-gated MOSFET. Current is reduced approximately 20× relative to Yb/Si$_3$N$_4$/Si S/D. (b) The output conductance at low V_D indicates a strong Schottky barrier at the source and drain.

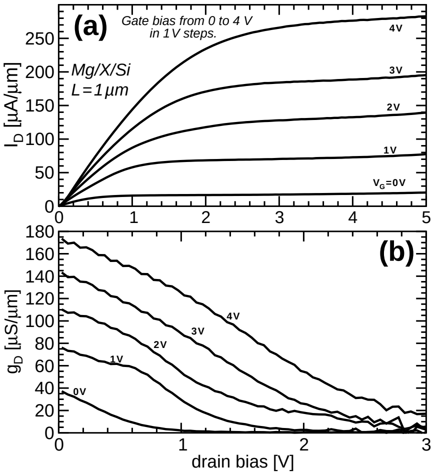

Fig. 10: (a) I_D versus V_D of Mg/Si$_3$N$_4$/Si S/D back-gated MOSFET. (b) Incremental conductance of same device. Results are comparable to those of the Yb/Si$_3$N$_4$/Si S/D FET, with indications of lower extrinsic series resistance between the S/D's and the probes.